Scheme and Syllabus
Of
Master of Technology
(VLSI Design Engineering)

Maharaja Ranjit Singh State Technical University, Bathinda
(Established by Govt. of Punjab vide Punjab Act No. 5 of 2015 and Section 2(f) of UGC)
## SCHEDULE OF TEACHING AND EXAMINATION FOR M.TECH. VLSI DESIGN

### 1st Semester

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<th>Subject Code</th>
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<th>Schedule of Teaching</th>
<th>Schedule of Examination</th>
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<tr>
<td>VL-511</td>
<td>Semiconductor Devices</td>
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## SCHEDULE OF TEACHING AND EXAMINATION FOR M.TECH. VLSI DESIGN
### 2ND SEMESTER

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<td>VL-521</td>
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<td>VL-522</td>
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<td>VL-523</td>
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<td>Testing and Fault Tolerance</td>
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<td><strong>Grand total</strong></td>
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## SCHEME OF TEACHING AND EXAMINATION FOR M.TECH. VLSI DESIGN

### List of Electives

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<td>VL-E1</td>
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<td>Sensor Technology and MEMS</td>
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M. Tech. (VLSI Design)

Core Subjects (10)

Semester-I

VL-511: Semiconductor Devices
VL-512: VLSI Design Concepts
VL-513: Hardware Description Languages
VL-514: VLSI Technology
VL-515: Design of Analog/Mixed Mode VLSI Circuits

Practical:

VL-516: VLSI Design - LAB
VL-517: Hardware Description Languages – LAB

Semester-II

VL-521: Advanced Digital Signal Processing
VL-522: ASIC Design And FPGAs
VL-523: Memory Design and Testing
VL-524: Embedded Systems
VL-525: Testing and Fault Tolerance

Practical:

VL-526: Designing with FPGAs - LAB
VL-527: Digital Signal Processing And Embedded System - LAB

Electives (2 out of 4)

E1 : System on Chip (SOC)
E2 : RF Design
E3 : Process & Device Characterization and measurements
E4 : Sensor Technologies and MEMS


MOSFET Modeling : Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect. Circuit models for MOS devices

Passive devices like resistors and capacitors, their non-idealities


Texts / References

VLSI Design Concepts:

Exam time: 3 Hours

Marks: 50


- CMOS Circuit And Logic Design: CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design.


- CMOS Sub System Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Texts / References

VL-513  Hardware Description Languages:  

- Basic concepts of hardware description languages.
- Hierarchy, Concurrency, logic and delay modeling.
- Structural, Data-flow and Behavioral styles of hardware description.
- Architecture of event driven simulators.
- Syntax and Semantics of VHDL.
- Variable and signal types, arrays and attributes.
- Operators, expressions and signal assignments.
- Entities, architecture specification and configurations.
- Component instantiation.
- Concurrent and sequential constructs.
- Use of Procedures and functions,
- Examples of design using VHDL.
- Syntax and Semantics of Verilog.
- Variable types, arrays and tables.
- Operators, expressions and signal assignments.
- Modules, nets and registers,
- Concurrent and sequential constructs.
- Tasks and functions,
- Examples of design using Verilog.
- Synthesis of logic from hardware description.
- Case Study and Mini Project

Texts / References

VLSI Technology:

- Environment for VLSI technology: clean room and safety requirements, Wafer cleaning process and wet chemical etching techniques

- Impurity incorporation: solid-state diffusion modeling and technology, Ion implantation: modeling, technology and damage annealing; Characterization of impurity profiles

- Oxidation: kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; high K and low K dielectrics for ULSI.

- Lithographic techniques: Photolithography techniques for VLSI/ULSI; Mask generation.

- Chemical Vapour deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; epitaxial growth of silicon; modeling and technology.

- Metalisation techniques: evaporation and sputtering techniques. Failure mechanisms in metal interconnects; multilevel Metalisation schemes.

- Masking Sequence and Process flow for MOS and BIPOLAR Devices

- Topological Design rules

Text/References

- Streetman,” VLSI Technology”.
Design of Analog/ Mixed Mode VLSI Circuits:


Text/References

- Greogorian & Tames, “ Analog Integrated Circuit For Switched Capacitor Circuit “
VL-516 VLSI Design - LAB

- NMOS Inverter
  Depletion and Enhancement Mode Circuit Simulation and Adjustment of $V_h$ VLSI $V_m$ parameters for NMOS inverter.

- CMOS Inverter
  Circuit Simulation, adjustment of $W / L$ ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners).
  Layout of CMOS Inverter, Extraction of parasitics and back annotation and related modifications in circuit parameters and layout.

- Current Source / Mirror
  Circuit simulation of current Mirror using BJT and MOS (Simple, Wilson and Widler configurations) study and modifications to improve power and load regulation.
  Layout of CMOS Current Mirror.

- 8 Bit shift register cell
  Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

- Differential Amplifier
  Study of specifications of Differential amplifier and Design considerations. Study of input loading and biasing techniques.
VL –517 Hardware Description Language – LAB:

- **2 Bit-Counter**

The purpose of this lab is to write a HDL description of 2-bit counter as a finite state machine (FSM). The 2-bit counter has several inputs such as clk, rst, enable, load, ... and should be able to reset, accept an input, count-up or count-down, etc...

- **Parallel to Serial Converter**

The purpose of this lab is to write a HDL description of a parallel to serial converter as an FSMD. The parallel to serial converter will accept an eight-bit number and send one bit of data over the data line per clock cycle. There is also a go bit, which tells the converter to start transmitting data.

- **VHDL Calculator**

The purpose of this lab is to implement a finite state machine in VHDL to perform simple calculations like addition, subtraction, and multiplication.

- **A Simplified HDL UART**

In this lab the students design a UART to send data to the PC.

- **I²C Bus Lab**

HDL implementation of I²C bus protocol

- **Design Of A Hardware Multiplier**

In this lab students are going to implement hardware multiplier using Sequential Circuit Components.

- **ALU Design**

The purpose of this lab is to build a 4/8-bit ALU. The ALU is written behaviorally. It should take in two numbers and be able to add the numbers, subtract the numbers, NOR the numbers, or NAND the numbers.
VL – 521

Advanced Digital Signal Processing:

Examin time : 3 Hours
Marks : 50


- Design of digital filters: introduction to filter design, types of digital filters, choosing between, fir and iir filters, filter design steps, effect of finite register length in filter design, realization of iir digital filters and fir digital filter, design of iir filters from continuous time filters, design of fir filters by windowing.

- Digital signal processors: general and special purpose digital signal processors, computer architecture for signal processing, selecting digital signal processors, architecture and programming of ADSP 2181 processor.


- Linear estimation and predication: maximum likelihood criterion efficiency of estimator, least mean squared error criterion, recursive estimators, and linear predcations.

- Multirate digital signal processing: Mathematical description of change of sampling rate, interpolation and decimation, continuous time model, direct digital domain approach, interpolation and decimation by an integer factor, single and multistage realization, applications of sub band coding.


- Introduction to DSP ASIC Design, Configurable Logic for Digital Signal Processing, Design Methodology for DSP, VLSI Implementation of DSP Processors

Text/Reference

- Proakes Manolakis , " Digital Signal Processing principles, algorithms, and applications", Prentice Hall India
- ADSP 2181 manuals
- Keshab K. Parhi, " VLSI DSP Systems; Design & implementation", Wiley InterScience Publishers
VL-522 ASIC Design and FPGA:

Exam time : 3 Hours
Marks : 50

- Introduction To ASICS, CMOS Logic And ASIC Library Design
  Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture.

- Review of VHDL/Verilog: Entities and architectures

- Programmable Asics, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells
  Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

- Programmable ASIC Interconnect, Programmable ASIC Design Software And Low Level Design Entry

- ASIC Construction, Floor Planning, Placement And Routing
  System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

- Design using Xilinx family FPGA

Text/References

- Skahill, Kevin," VHDL for Programmable Logic", Addison-Wesley, 1996
Memory Design and Testing:

Random Access Memory Technologies
Static Random Access Memories (SRAMs):
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.
Dynamic Random Access Memories (DRAMs):
DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BiCMOS DRAMs-Soft Error Failures in DRAM-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Nonvolatile Memories
Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance

Semiconductor Memory Reliability And Radiation Effects
General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.

Advanced Memory Technologies And High-Density Memory Packaging Technologies
Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Text/Reference
- Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.
- Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S)
VL- 524  Embedded Systems:

- Introduction And Examples Of Embedded Systems, Concept Of Embedded System Design: Design challenge, Processor technology, IC technology, Design technology, Trade-offs

- Custom single purpose processor hardware, general-purpose processor: introduction, basic architecture, operation, super-scalar and VLSIW architecture, application specific instruction set processors (ASIPS), microcontrollers, digital signal processors, selecting a microprocessor.

- Memory: Introduction, Memory write ability, Storage performance, Tradeoffs, Common memory types Memory hierarchy and cache

- AVR 8515 microcontroller: Architecture and Programming in assembly and C.

- Interfacing Analog and digital blocks: Analog-to-Digital Converters (ADCs), Digital-to-Analog, Converters (DACs), Communication basics and basic protocol concepts, Microprocessor interfacing: I/O addressing, Port and Bus based, I/O, Memory mapped I/O, Standard I/O interrupts, Direct memory access, Advanced communication principles parallel, serial and wireless, Serial protocols I^2C, Parallel protocols PCI bus, Wireless protocol IrDA, blue tooth.

- Different peripheral devices: Buffers and latches, Crystal, Reset circuit, Chip select logic circuit, timers and counters and watch dog timers, Universal asynchronous receiver, transmitter (UART), Pulse width modulators, LCD controllers, Keypad controllers.

- Design tradeoffs due to thermal considerations and Effects of EMI/ES etc.

- Software aspect of embedded systems: Challenges and issues in embedded software development, Co-design

- Embedded software development environments: Real time operating systems, Kernel architecture: Hardware, Task/process control subsystem, Device drivers, File subsystem, system calls, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin, priority based scheduling, Context switch: Task synchronization: mutex, semaphore, Timers, Types of embedded operating systems, Programming languages: assembly languages, high level languages

- Development for embedded systems: Embedded system development process, Determine the requirements, Design the system architecture, Choose the operating system, Choose the processor, Choose the development platform, Choose the programming language, Coding issues, Code optimization, Efficient input/output, Testing and debugging, Verify the software on the host system, Verify the software on the embedded system
TEXT /REFERENCE

- Frankvahid/Tony Givargis, “Embedded System Design- A unified Hardware/software Introduction”.
- Dreamteach Software team,"Programming for Embedded Systems"
- AVR 8515 manual
- J.W. Valvano, "Embedded Microcomputer System: Real Time Interfacing"
VL-525        Testing and Fault Tolerance:

Exam time : 3 Hours
Marks : 50

- Physical Faults and their Modelling
- Stuck-at Faults, Bridging Faults
- Fault Collapsing; Fault Simulation
- Deductive, Parallel, and Concurrent Fault Simulation Critical Path Tracing
- ATPG for Combinational Circuits: D- Algorithm, Boolean Difference, Podem
- Random, Deterministic and Weighted Random Test Pattern Generation Aliasing and its Effect on Fault Coverage
- PLA Testing, Cross Point Fault Model and Test Generation
- Memory Testing - Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests
- Delay Faults; ATPG for Sequential Circuits
- Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board Level Testing
- BIST and Totally Self checking Circuits
- System level Diagnosis; Introduction
- Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes
- Reconfiguration Techniques
- Yield Modelling Reliability and effective area utilization.

Text/References
VL-526  Designing with FPGAs - LAB

- **USART**
  Designing the Specifications and circuit of a USART.
  Implementation of a USART on FPGA.

- **Multiplexed Display Controller**
  Designing the Specifications and circuit of a Multiplexed Display Controller (MDC)
  Implementation of a Multiplexed Display Controller on FPGA.

- **CRT Controller**
  Designing the Specifications and circuit of a CRT Controller.
  Implementation of a CRT Controller on FPGA.

- **I/O Port Expander**
  Designing the Specifications and circuit of I/O port expander.
  Implementation of I/O Expander on FPGA.

- **Scanned Keyboard Controller**
  Designing the Specifications and circuit of a Scanned Keyboard Controller.
  Implementation of a Scanned Keyboard Controller on FPGA.

- **Filter Implementation using MAC**
  Designing the Specifications and circuit of a Filter Implementation using MAC.
  Implementation of a MAC on FPGA.
VL-527 Digital Signal Processing and Embedded System LAB:

Digital Signal Processing – LAB

- Accessing Memory-Mapped registers and Non-Memory-Mapped Registers of ADSP 2181 In C
- Programming The ADSP-21xx Timer In C
- FFT implementation using ADSP 2181
- Digital filter design using ADSP 2181.
- Powering up and programming the AD1847 using an ADSP-2100 Family DSP.
- Implementation of adaptive filters using ADSP 2181.

Embedded Systems - LAB

- Decimal Counter and Multiplexing the Output
  The purpose of this lab is to implement a decimal counter, which counts from 0 to 99. The students will be required to write a program for the AVR 8515 micro-controller.
- Watchdog Timer
  In this lab the students will design a hardware watchdog timer. They are ment to write a buggy program in order to test their WDT. The 8515 program should perform some computation, e.g., write 1, 2, 3 ... to the LED and at some point enter an infinite loop. During normal operation, the 8515 program must periodically (up to 254 second long cycles) write to the WDT's initial value register to avoid unnecessary resets.
- AVR microcontroller UART in C
  Implement AVR microcontroller UART in C
- Implementation of simple calculator using AVR 8515
  Implement a simple calculator using AVR 8515 microcontroller with keyboard and LCD display interface.
- Analog to Digital Conversion
  To be able to implement analog to digital conversion using the ADC0804LCN 8-bit A/D convertor. You will design a circuit and program the chip so that when an analog signal is given as input, the equivalent digital voltage is displayed on an LCD display.
- Implementing SPI bus Using AVR 8515
  The students are required to implement I2C serial communication using AVR 8515.
- Digital Filters with AVR
Implement digital filters using low cost microcontroller from AVR series.

- **Converting 8-bit LCD communication to 4-bit**

  Interface LCD with AVR 8515 using only 4 microcontroller pins

- **IR Remote Control Receiver**

  In this lab students are required to design and implement IR remote control receiver using AVR 8515 microcontroller.

- **Step Motor Controller**

  In this lab students are meant to implement a compact size and high-speed interrupt driven step motor controller.

- **A Temperature Monitoring and Acquisition System with LCD Output and memory interface**

  Implement this using the SDK- 500 Kit for AVR.
System on Chip (SoC):

- System on Chip Technology Challenges
- System On a Chip (SOC) components.
- SoC Design Methodology
- Parameterized Systems-on-a-Chip
- System-on-a-chip Peripheral Cores
- SoC and interconnect centric Architectures
- System level design representations and modeling languages.
- Target architecture models.
- Intra-chip communication.
- Graph partitioning algorithms.
- Task time measurement.
- Interconnect latency modeling.
- Back annotation of lower level timing to high-level models.
- Synthesis of SOC components.
- System Level, Block Level and Hardware/Software Co-verification
- SOC components: emulation, co-simulation, Physical Verification.

Text/References
- Wayone Wolf," Modern VLSI Design: SOC Design"
VL-E2 531 RF Design:

- Introduction to RF Electronics.
- Basic concepts in RF design.
- MOS Review
- Path Loss
- Small Signal Model
- Receiver Design
- RF Transreceivers
- Low Noise RF amplifiers and Mixers.
- RF Power amplifiers.
- RF Oscillators.

Text/References

- Behzad Razavi, “RF Microelectronics”, Pearson Education.
- Reinhold Ludwig, Paul Bretchko, “RF Circuit Design: Theory & Applications ”
VL-E3  

Process and Device Characterization & Measurements:

Exam time : 3 Hours  
Marks : 50

- Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR
- Material and Impurity Characterization: SIMS, XRD, EDAX
- Electrical Characterization: Four-probe technique, Hall effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements
- Process and SPICE model parameter Extraction.

Text/References

- Schroder, “Semiconductor Material And Device Characterization”
VL-E4 Sensor Technologies and MEMS:

Exam time: 3 Hours
Marks: 50

- Sensors types and classification – mechanical, acoustic, magnetic, thermal, chemical, radiation and biosensors.
- Microsensors.
- Sensors based on surface-acoustic wave devices.
- Micromachining techniques
- MEMS for automotive, communication and signal processing applications.
- Modeling and simulation of microsensors and actuators.
- Sensors and smart structures.
- Micro-opto-electro-mechanical sensors and system.

Text/References